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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,478	BRATT ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-33 and 35-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-33 and 35-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9, 11-33, and 35-50 have been considered. Claims 10 and 34 have been cancelled as per Applicant's request. Claims 1-2, 4-5, 11-12, 17, 25, 28, 29, 35-36, and 41 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 03 March 2006; Extension of Time for 1 Month as received on 03 March 2006; and Amendment as received on 03 March 2006.

Claim Objections

3. Claims 20 and 28 are objected to because of the following informalities:

   a. Referring to claim 20, please correct the claim from "A method as in claim 11 the look-up memory..." to read --A method as in claim 11 wherein the look-up memory...--.

   b. Referring to claim 28, please correct the claim from "...wherein the the replacing is performed..." to read -- wherein the [[the]]replacing is performed...--.

4. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 11-24 and 35-48 are rejected under 35 U.S.C. 102(e) as being taught by Sazegari, U.S. Patent Number 6,446,198 (herein referred to as Sazegari).

7. Referring to claims 11 and 35, taking claim 11 as exemplary, Sazegari has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

b. Receiving a first vector having a plurality of numbers (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

c. Partitioning look-up memory into a plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

d. Looking up simultaneously a plurality of elements of a second vector from the plurality of look-up tables, each of the plurality of elements being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

e. Wherein the partitioning and the looking-up operations are performed in response to the microprocessor receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

8. Claim 35 is nearly identical to claim 11, differing in it's a method being comprised upon a machine-readable medium, but encompassing the same scope as claim 11. Therefore, claim 35 is rejected for the same reasons as claim 11.

9. Referring to claims 12 and 36, taking claim 12 as exemplary, Sazegari has taught a method as in claim 11 wherein the receiving the first vector having a plurality of numbers comprises partitioning a string of bits into a plurality of segments to generate the plurality of numbers (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

10. Referring to claims 13 and 37, taking claim 13 as exemplary, Sazegari has taught a method as in claim 12 wherein the single instruction specifies format information in which the plurality of numbers are stored in the string of bits (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

11. Referring to claims 14 and 38, taking claim 14 as exemplary, Sazegari has taught a method as in claim 11

a. Wherein the look-up memory comprises a plurality of look-up units (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6), and

b. Wherein said partitioning look-up memory comprises configuring the plurality of look-up units into the plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

12. Referring to claims 15 and 39, taking claim 15 as exemplary, Sazegari has taught a

method as in claim 12 wherein the string of bits is received from an entry of a register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

13. Referring to claims 16 and 40, taking claim 16 as exemplary, Sazegari has taught a method as in claim 15 wherein the single instruction specifies an index of the entry (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

14. Referring to claims 17 and 41, taking claim 17 as exemplary, Sazegari has taught a method as in claim 11 further comprising storing the second vector having the plurality of elements in an entry of a register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

15. Referring to claims 18 and 42, taking claim 18 as exemplary, Sazegari has taught a method as in claim 17 wherein the single instruction species an index of the entry (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

16. Referring to claims 19 and 43, taking claim 19 as exemplary, Sazegari has taught a method as in claim 17 wherein the single instruction specifies format information in which the plurality of elements are stored in the entry (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

17. Referring to claims 20 and 44, taking claim 20 as exemplary, Sazegari has taught a method as in clam 11 the look-up memory comprises a plurality of look-up units, and

a. Wherein said partitioning look-up memory comprises configuring the plurality of

look-up units into the plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6); and

b. Wherein each of the plurality of look-up units comprises 256 8-bit entries (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

18. Referring to claims 21 and 45, taking claim 21 as exemplary, Sazegari has taught a method as in claim 11 wherein the single instruction specifies a total number of entries contained in each of the plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

19. Referring to claims 22 and 46, taking claim 22 as exemplary, Sazegari has taught a method as in claim 21 wherein the total number of entries is one of:

a. 256 (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

b. 512; and

c. 1024.

20. Referring to claims 23 and 47, taking claim 23 as exemplary, Sazegari has taught a method as in claim 11 wherein the single instruction specifies a total number of bits used by each entry contained in the plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

21. Referring to claims 23 and 48, taking claim 24 as exemplary, Sazegari has taught a method as in claim 21 wherein the total number of bits is one of:

a. 8 (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

b. 16; and

c. 24.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 1-9, 25-33, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sazegari, U.S. Patent Number 6,446,198 (herein referred to as Sazegari) in view of Barry et al., U.S. Patent Number 6,397,324 (herein referred to as Barry) and in further view of Priem, U.S. Patent Number 5,768,628 (herein referred to as Priem).

24. Referring to claims 1 and 25, taking claim 1 as exemplary, Sazegari has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

b. Receiving a first vector having a first plurality of numbers and a second vector having a second plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables (Sazegari Abstract; column 2, lines 17-43;

column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6); and

c. Operating on simultaneously the plurality of entries in the plurality of look-up tables with the second plurality of numbers (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6); and

d. Wherein the receiving and the operating operations are performed in response to the microprocessor receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

25. Sazegari has not taught the operation being replacing. Barry has taught replacing data simultaneously in the look-up tables (Barry Col.9 lines 41-62 and Col.12 lines 14-27). A person of ordinary skill in the art at the time the invention was made, and as taught by Barry, would have recognized the simultaneous storing of data in a look-up table increases efficiency for processing compressed data (Barry column 1, lines 66-67 and column 2, lines 40-41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the store operation of Barry in the device of Sazegari to improve compressed data processing efficiency.

26. In addition, Sazegari has not taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit. Priem has taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit (Priem Abstract; column 6, line

45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4). A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improve processor speed and efficiency.

27. Claim 25 is nearly identical to claim 1, differing in its method being comprised upon a machine-readable medium, but encompassing the same scope as claim 1. Therefore, claim 25 is rejected for the same reasons as claim 1.

28. Referring to claims 2 and 26, taking claim 2 as exemplary, Sazegari has taught a method as in claim 1, wherein the first vector having the first plurality of numbers are is received from a first entry in a register file; and the second vector having the second plurality of numbers are is received from a second entry in the register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

29. Referring to claims 3 and 27, taking claim 3 as exemplary, Sazegari has taught a method as in claim 2 wherein the single instruction specifies indices of the first and second entries in the register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

30. Referring to claims 4 and 28, taking claim 4 as exemplary, Sazegari has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6); and

b. Operating on at least one entry in at least one of a plurality of look-up units in a microprocessor unit with at least one number (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

c. Wherein the operating is performed in response to the microprocessor receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

31. Sazegari has not taught the operation being replacing. Barry has taught replacing data simultaneously in the look-up tables (Barry Col.9 lines 41-62 and Col.12 lines 14-27). A person of ordinary skill in the art at the time the invention was made, and as taught by Barry, would have recognized the simultaneous storing of data in a look-up table increases efficiency for processing compressed data (Barry column 1, lines 66-67 and column 2, lines 40-41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the store operation of Barry in the device of Sazegari to improve compressed data processing efficiency.

32. Sazegari has not taught using

a. The instruction having an identity number code that specifies a DMA controller; and

b. Using the Direct Memory Access (DMA) controller.

33. Priem has taught using

a. The instruction having an identity number code that specifies a DMA controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4); and

b. Using the Direct Memory Access (DMA) controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4).

34. In regards to Priem, the wave tables are transferred vie the sound card's sound generation controller's DMA in response to CPU commands, e.g. instructions, that identify the sound tables need to be loaded. In other words, the CPU commands to transfer the sound tables identify and command the sound controller, and in turn the DMA controller, to transfer the tables. A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improve processor speed and efficiency.

35. Claim 28 is nearly identical to claim 4, differing in its method being comprised upon a machine-readable medium, but encompassing the same scope as claim 4. Therefore, claim 28 is rejected for the same reasons as claim 4.

36. Referring to claims 5 and 29, taking claim 5 as exemplary, Sazegari has taught a method for execution by a microprocessor in response to receiving a single instruction, the method

comprising:

a. Receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6); and

b. Operating on at least one entry for each of a plurality of look-up units in a microprocessor with a plurality of numbers (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6);

c. Wherein the operating is performed in response to the microprocessor receiving the single instruction (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

37. Sazegari has not taught the operation being replacing. Barry has taught replacing data simultaneously in the look-up tables (Barry Col.9 lines 41-62 and Col.12 lines 14-27). A person of ordinary skill in the art at the time the invention was made, and as taught by Barry, would have recognized the simultaneous storing of data in a look-up table increases efficiency for processing compressed data (Barry column 1, lines 66-67 and column 2, lines 40-41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the store operation of Barry in the device of Sazegari to improve compressed data processing efficiency.

38. Sazegari has not taught using

a. The instruction having an identity number code that specifies a DMA controller; and

b. Using the Direct Memory Access (DMA) controller.

39. Priem has taught using

a. The instruction having an identity number code that specifies a DMA controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4); and

b. Using the Direct Memory Access (DMA) controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4).

40. In regards to Priem, the wave tables are transferred vie the sound card's sound generation controller's DMA in response to CPU commands, e.g. instructions, that identify the sound tables need to be loaded. In other words, the CPU commands to transfer the sound tables identify and command the sound controller, and in turn the DMA controller, to transfer the tables. A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improve processor speed and efficiency.

41. Claim 29 is nearly identical to claim 5, differing in its method being comprised upon a machine-readable medium, but encompassing the same scope as claim 5. Therefore, claim 29 is rejected for the same reasons as claim 5.

42. Referring to claims 6 and 30, taking claim 6 as exemplary, Sazegari has taught a method

as in claim 5 wherein a single index encoded in the instruction specifies a location of the at least one entry in the plurality of look-up units (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

43. Referring to claims 7 and 31, taking claim 7 as exemplary, Sazegari has taught a method as in claim 5 wherein a single index encoded in the instruction specifies a total number of the at least one entry for each of a plurality of look-up units (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

44. Referring to claims 8 and 32, taking claim 8 as exemplary, Sazegari has taught a method as in claim 5 wherein a source address of the plurality of numbers in host memory is specified in an entry of a register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

45. Referring to claims 9 and 33, taking claim 9 as exemplary, Sazegari has taught a method as in claim 8 wherein the single instruction specifies an index of the entry in the register file (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

46. Referring to claim 49, Sazegari has taught a method as in claim 5 wherein the at least one entry for each of the plurality of look-up units comprises a plurality of entries for each of the plurality of look-up units (Sazegari Abstract; column 2, lines 17-43; column 4, lines 5-19, 26-32, 41-46, and 59-63; Figure 2, Figure 4; and Figure 6).

47. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sazegari, U.S. Patent Number 6,446,198 (herein referred to as Sazegari), as applied to claim 11 above, and in further view of Priem, U.S. Patent Number 5,768,628 (herein referred to as Priem). Sazegari has

not taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit. Priem has taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4). A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improve processor speed and efficiency.

Response to Arguments

48. Applicant's arguments with respect to claims 1-9, 11-33, and 35-50 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

50. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

51. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
14 May 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100